VLSI CHIP TEST POWER REDUCTION

Abstract

LBIST and weighted LBIST tests are performed simultaneously on different portions of the tested object. This new test methodology and design change achieves the same test coverage and test time as the traditional test strategy with dramatic power reduction during test. It can be applied at wafer, chip, MCM, and system levels of test. Most importantly, it does not need new tools for support. Current test software will work as it does with the traditional test strategy. Scheduling the LBIST and weighted LBIST tests in the same test session reduces the overall power consumption because weighted LBIST testing consumes much less power than flat LBIST testing. In the same test session, if some parts of the logic is tested using weighted LBIST while the others were tested using LBIST, the power consumed by the circuit element at any given time is reduced.